Intel® 848P Chipset

Thermal Design Guide

For the Intel® 82848P Memory Controller Hub (MCH)

August 2003

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Revision History

Revision	Description	Date
-001	• Initial Release.	August 2003

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1 Introduction

As the complexity of computer systems increase, so do power dissipation requirements. The additional power of next generation systems must be properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting, and/or passive heatsinks.

The objective of thermal management is to ensure that the temperatures of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors, or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component. The goal of this document is to provide an understanding of the operating limits of the Intel® 848P chipset Memory Controller Hub (82848P MCH), and discuss a reference thermal solution.

The simplest and most cost-effective method is to improve the inherent system cooling characteristics of the MCH through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document presents the conditions and requirements to properly design a cooling solution for systems that implement the 848P chipset. Properly designed solutions provide adequate cooling to maintain the chipset MCH case temperature at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the case to local-ambient thermal resistance. By maintaining the MCH case temperature at or below those recommended in this document, a system designer can ensure the proper functionality, performance, and reliability of this chipset.

1.1 Terminology

Term	Description
BGA	Ball Grid Array. A package type defined by a resin-fiber substrate where a die is mounted, bonded, and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
Intel® ICH5	Intel® I/O Controller Hub 5. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA, and/or other legacy functions.
MBGA	Mini Ball Grid Array. A smaller version of the BGA with a ball pitch of 1.00 mm [0.039 in].
MCH	Memory Controller Hub. The chipset component that contains the processor and memory interface.

Term	Description
T_A	The measured ambient temperature locally to the component of interest. The ambient temperature should be measured just upstream of airflow for a passive heatsink or at the fan inlet for an active heatsink.
T_C	The measured case temperature of a component. For processors, it is measured at the geometric center of the integrated heat spreader (IHS). For other component types, it is generally measured at the geometric center of the die or case.
$T_{C\text{-}MAX}$	The maximum case/die temperature with an attached heatsink. This temperature is measured at the geometric center of the top of the package case/die.
$T_{C\text{-}MIN}$	The minimum case/die temperature with an attached heatsink. This temperature is measured at the geometric center of the top of the package case/die.
TDP	Thermal Design Power is specified as the highest sustainable power level of most or all of the real applications expected to be run on the given product, based on extrapolations in both hardware and software technology over the life of the component. Thermal solutions should be designed to dissipate this target power level.
TIM	Thermal Interface Material: thermally conductive material installed between two surfaces to improve heat transfer and reduce interface contact resistance.
lfm	Linear Feet per Minute. Unit of airflow speed.
Ψ_{CA}	Case-to-ambient thermal characterization parameter (Psi). A measure of thermal solution performance using total package power. Defined as $(T_C - T_A)$ / Total Package Power. Heat source size should always be specified for Ψ measurements.
WSHS	Wave Solder Heatsink. A heatsink that is installed to a motherboard via wave solder process. Pins are fixed to the heatsink base and are held in place on the motherboard by solder. There are no associated retention clips or retention anchors.

1.2 Reference Documents

Document	Document Number / Location
Intel® 848P Chipset: Intel® 82848P Memory Controller Hub (MCH) Datasheet	253575
Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5 R (ICH5R) Thermal Design Guide	http://developer.intel.com/design/chipsets/designex/252673.htm
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet	http://developer.intel.com/design/pentium4/datashts/298643.htm
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines Design Guide	http://developer.intel.com/design/pentium4/guides/252161.htm
Various System Thermal Design Suggestions	http://www.formfactors.org

2 Product Specifications

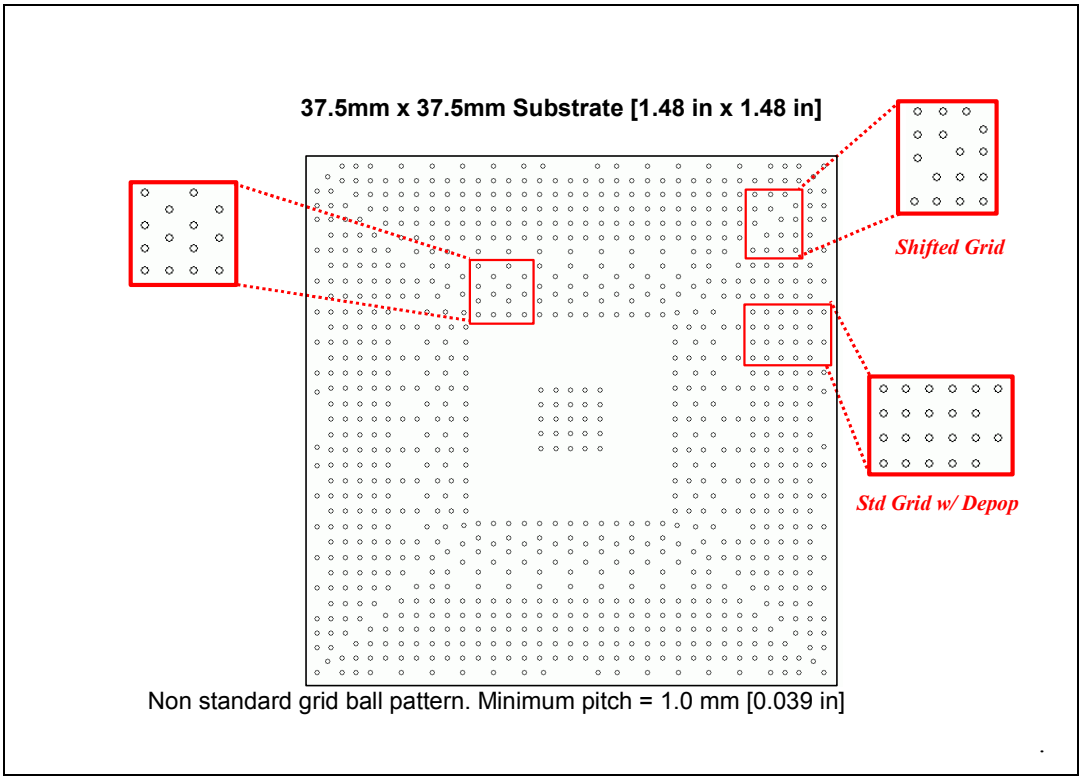
2.1 Package Description

The MCH is available in a 37.5 mm [1.48 in] x 37.5 mm [1.48 in] Flip Chip Ball Grid Array (FC-BGA) package with 932 solder balls. The die size is currently 9.73 mm [0.383 in] x 9.73 mm [0.383 in] and is subject to change. A mechanical drawing of the package is shown in Figure 14, Appendix A.

2.1.1 Non-Grid Array Package Ball Placement

The MCH package uses a "balls anywhere" concept. Minimum ball pitch is 1.0 mm [0.039 in], but ball ordering does not follow a 1mm grid. Board designers should ensure correct ball placement when designing for the non-grid array pattern. For exact ball locations relative to the package, refer to the *Intel® 848P Chipset Datasheet.*

Figure 1. MCH Non-Grid Array



2.2 Thermal Specifications

To ensure proper operation and reliability of the MCH, the temperature must be at or below the maximum value specified in Table 1. System and component level thermal enhancements are required to dissipate the heat generated and maintain the MCH within specifications. Chapter 3 provides the thermal metrology guidelines for case temperature measurements. The MCH should also operate above the minimum case temperature specification listed in Table 1.

Table 1. Intel® 82848P MCH Case Temperature Specifications

Parameter	Value	Notes
$T_{C\text{-}MAX}$	99°C	1
$T_{C\text{-}MIN}$	0 °C	1

NOTES:
1. Thermal specifications assume an attached heatsink is present.

2.3 Thermal Design Power (TDP)

Thermal design power (TDP) is the estimated power dissipation of the MCH based on normal operating conditions including V_{CC} and $T_{C\text{-}MAX}$ while executing real worst-case power intensive applications. This value is based on expected worst-case data traffic patterns and usage of the chipset and does not represent a specific software application. TDP attempts to account for expected increases in power due to variation in chipset current consumption due to silicon process variation, processor speed, DRAM capacitive bus loading, and temperature. However, since these variations are subject to change, the TDP cannot guarantee that all applications will not exceed the TDP value.

The system designer must design a thermal solution for the MCH such that it maintains T_C below $T_{C\text{-}MAX}$ for a sustained power level equal to TDP. The TDP value can be used for thermal design if the chipset thermal protection mechanisms are enabled. Intel chipsets provide a hardware-based fail-safe mechanism incorporated to keep the product temperature in specification in the event of unusually strenuous usage above the TDP power.

The MCH provides a hardware-based mechanism to reduce MCH power by limiting the traffic that occurs to certain interfaces. Traffic limits are programmed into the chipset registers during system boot as part of the Intel supplied BIOS reference code.

2.3.1 Methodology

2.3.2 Application Power

Designing to the TDP can ensure a particular thermal solution can meet the cooling needs of future applications. Testing with currently available commercial applications has shown they may dissipate power levels below the published TDP specification in Section 2.3.3. Intel strongly recommends that thermal engineers design to the published TDP specifications to develop a robust thermal solution that will meet the needs of current and future applications.

2.3.3 Specifications

The MCH dissipates the configuration specific Thermal Design Power value provided in Table 2. Note that actual power dissipated may differ from part to part due to normal manufacturing process variability. The leakage power of the device will vary from unit to unit. The TDP values account for leakage variation from unit to unit and system designers should design to the TDP specifications in Table 2. As a manufacturing process improves and the circuit density increases, the leakage power of the device increases. In general, the leakage is lower for the initial silicon than it is at the end of the product's life.

FC-BGA packages have minimal heat transfer capability into the board and therefore have minimal thermal capability without thermal solutions. Intel requires that system designers plan for an attached heatsink when using the MCH.

Table 2. Intel® 82848P MCH Thermal Design Power Specifications

Configuration	TDP Value
Single-channel / 2 DIMMs / 400 MHz DDR / 800 MHz FSB	8.1 W

2.4 Mechanical Specifications

Heatsinks that attach to the MCH via a retention mechanism should exert a load within the maximum static load specification listed in Table 3. During heatsink installation, care should be taken to avoid rocking the heatsink on the package die or exceeding the maximum transient compressive load in Table 3.

Table 3. MCH Mechanical Specifications

Parameter	Value	Notes
Maximum Static Compressive Load	133.4 N [30 lbf]	1
Maximum Transient Compressive Load	178 N [40 lbf]	2

NOTES:
1. A compressive load is defined as a uniform load applied normal to the die surface (downwards)
2. A transient compressive load is defined as a uniform load applied normal to the die surface (downwards) temporarily during heatsink installation.

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3 Thermal Metrology

The system designer must measure temperatures to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques of measuring chipset component case temperatures.

3.1 Case Temperature Measurements

To ensure functionality and reliability, the MCH is specified for proper operation when T_C is maintained at or below the maximum temperature listed in Table 2. The surface temperature at the geometric center of the die corresponds to T_C. Measuring T_C requires special care to ensure an accurate temperature reading.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heatsink base (if a heatsink is used). To minimize these measurement errors a thermocouple attach with a zero-degree methodology is recommended.

Although the basic metrology is the same for a clip-attached heatsink and a Wave Solder Heatsink (WSHS), the removal and replacement of the WSHS requires additional guidelines for accurate thermal measurements. Refer to the WSHS rework procedure in Section 4.3.3 for guidelines on installing a WSHS modified for a zero-degree attach. Physical modifications to a WSHS are identical to modifications for a clip-attached heatsink. Sections 3.1.1 details the modifications required to measure package case temperature using both clip-attached heatsinks and WSHS.

3.1.1 Thermocouple Attach Methodology

1. Mill a 3.3 mm [0.13 in] diameter hole centered on the bottom of the heatsink base. The milled hole should be approximately 1.5 mm [0.06 in] deep.
2. Mill a 1.3 mm [0.05 in] wide slot, 0.5 mm [0.02 in] deep, from the centered hole to one edge of the heatsink. The slot should be in the direction parallel to the heatsink fins (see Figure 3).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, make sure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 2).
6. Attach heatsink assembly to the MCH and route thermocouple wires out through the milled slot. For the Wave Solder Heatsink, refer to Section 4.3.3 for guidelines on proper heatsink removal and installation. Following the guidelines is critical to ensure an accurate and repeatable metrology.

Figure 2. Zero-Degree Angle Attach Methodology

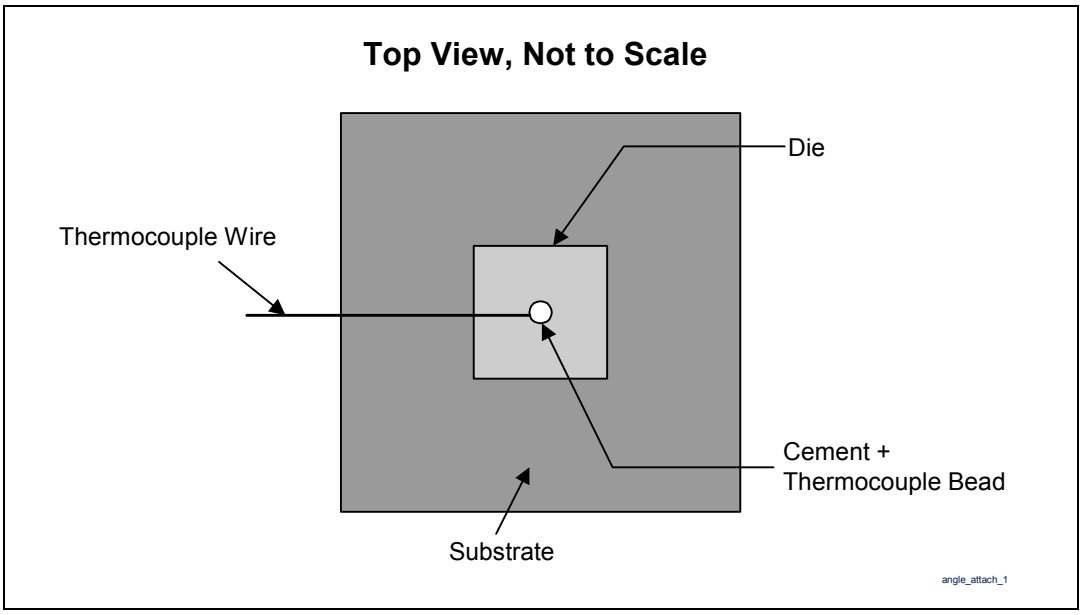
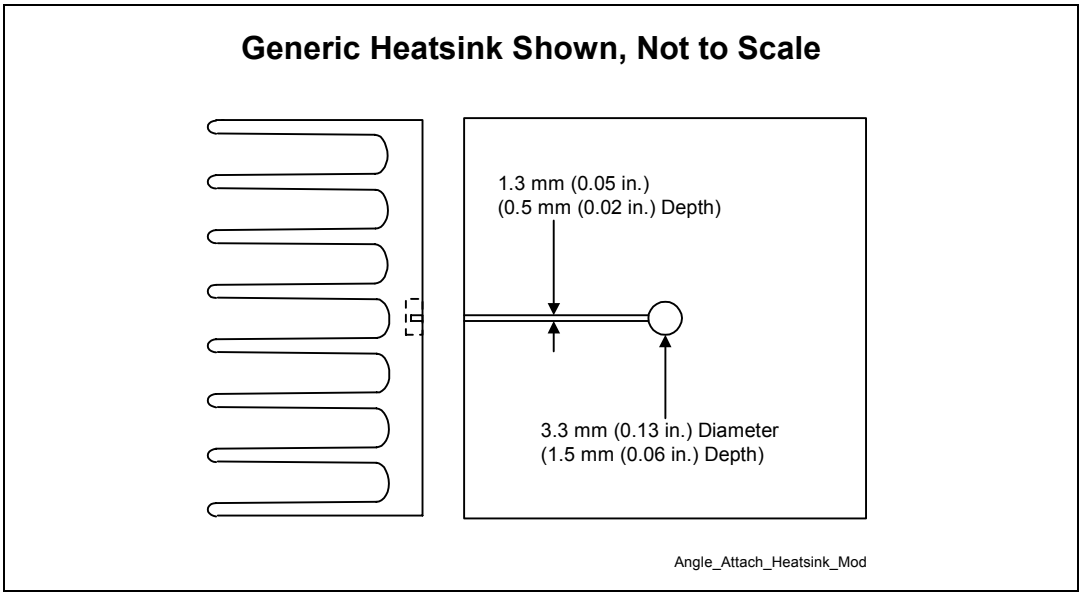


Figure 3. Zero-Degree Angle Attach Heatsink Modifications



3.2 Thermal Mechanical Test Vehicle

A Thermal Mechanical Test Vehicle (TMTV) is available for early thermal testing prior to the availability of actual silicon. The TMTV contains a heater die and can be powered up to a desired power level to simulate the heating of a MCH package. The TMTV also contains daisy chain functionality and can be used for mechanical testing. The TMTV needs to be surface mounted to a custom board designed to provide connectivity to the die heater and/or daisy chain depending on the needs of the user. The package ball connections are provided so the user may design and build a board to interface with the TMTV. Note that although the TMTV is designed to closely match the MCH package mechanical form and fit, it is recommended that final validation be performed with actual production material. The TMTV mechanical features, including die size, ball count, etc., may not reflect those of the final production package.

3.2.1 TMTV Daisy Chain Operation

The TMTV has alternating pins shorted together on the package to allow daisy chain functionality. When mounted to a complementary test board, entire rows or the entire package can be shorted together. Test points on the board can then facilitate the identification of any opens on the mounted package after any mechanical testing (shock, vibration, temperature cycling, etc.). Figure 4 shows a schematic of the internal package structures and Figure 5 shows an example of a complementary test board configuration.

Figure 4. TMTV Daisy Chain Structure

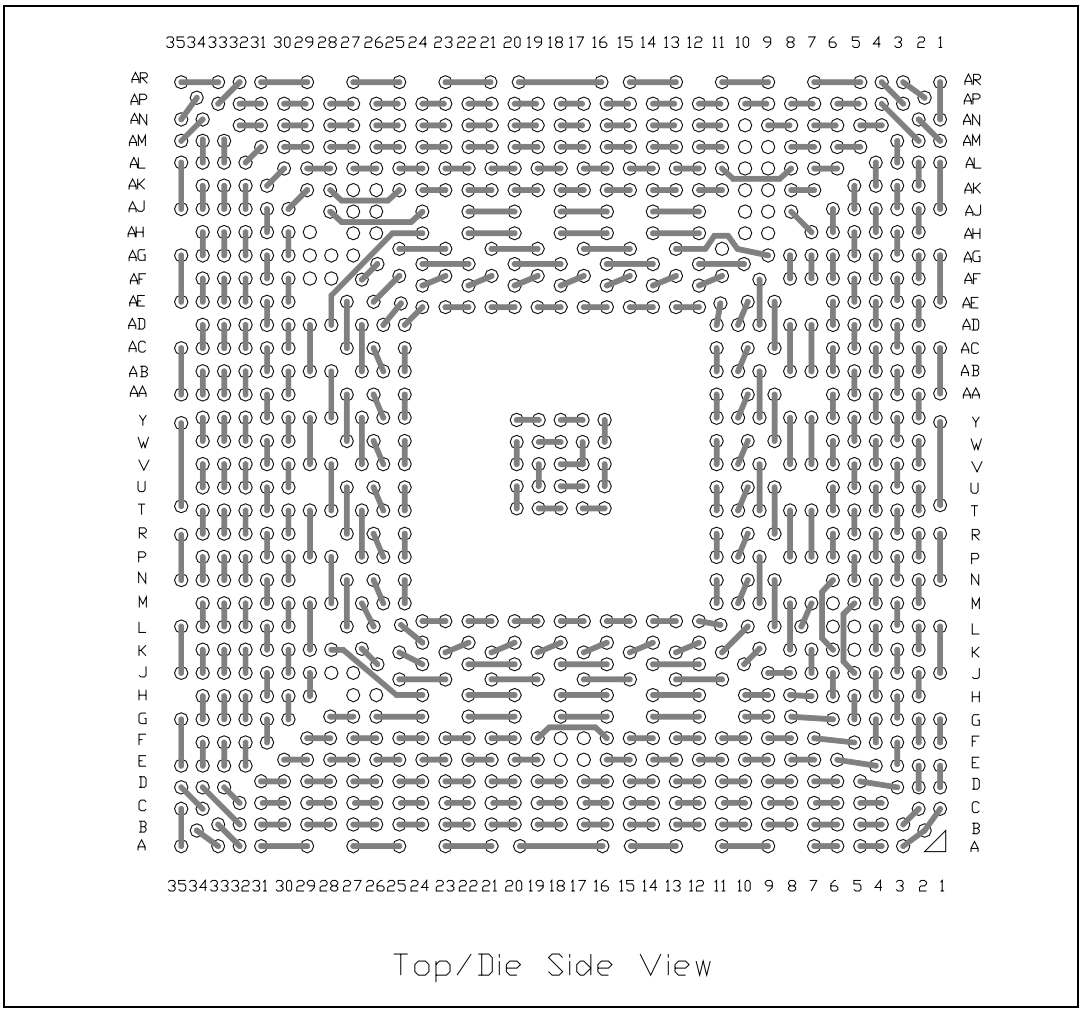
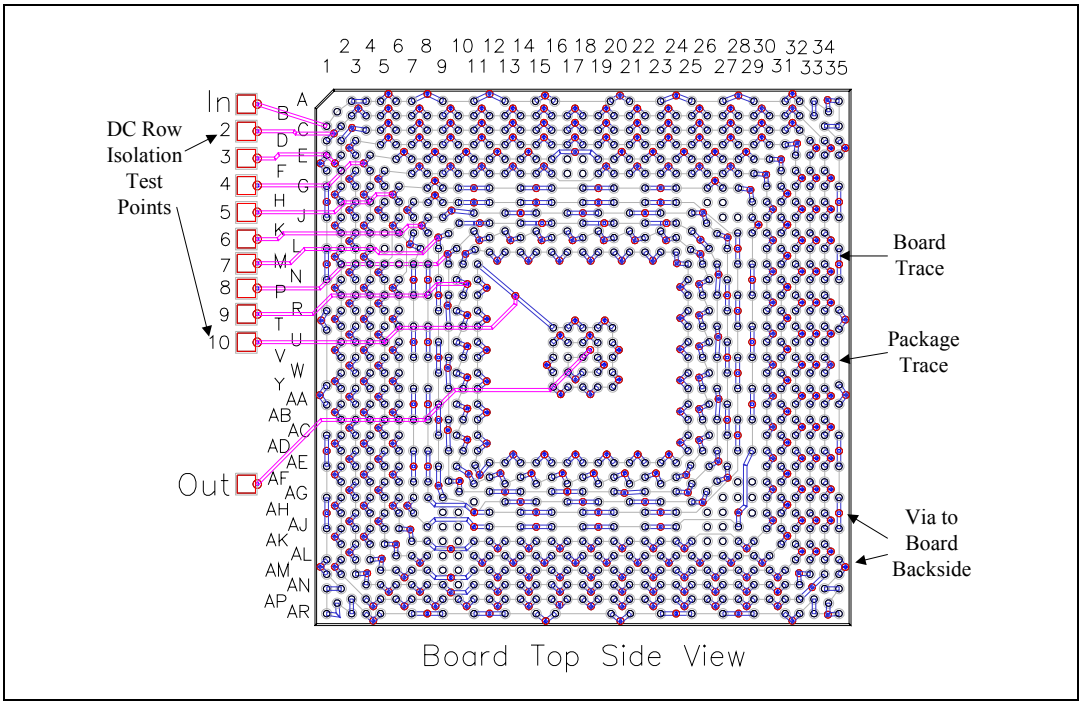


Figure 5. Example Complementary Test Board Connections



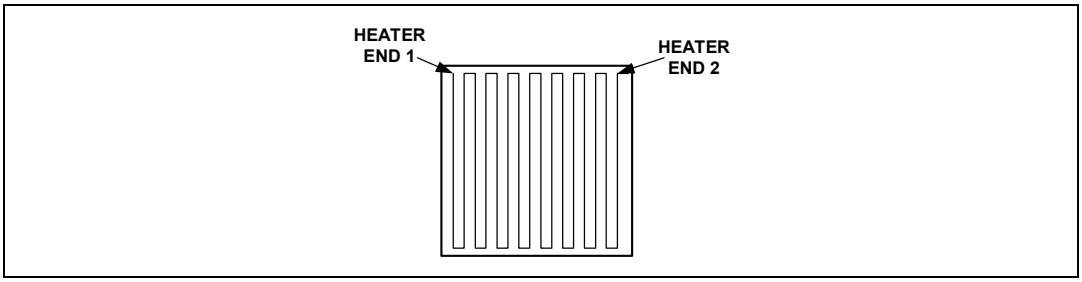
3.2.2 TMTV Thermal Operation

The heater located within the TMTV die should be accessed by connecting two sets of eight (8) solder balls to each side of a power supply in parallel. The heater consists of a resistor and the polarity of the power supply connections is arbitrary. The package balls to access the heater are identified in Table 4. Ball reference designations can be found in Figure 4 and Figure 5. A graphical representation of the die heater and its connections are shown in Figure 6.

Table 4. TMTV Heater Connections

Ball Designation	Connection
AK10, AM9, AL9, AM10, AL10, AG11, AK9, AN10	Heater End 1
AG28, AF28, AF29, AG27, AH27, AG29, AH26, AH29	Heater End 2

Figure 6. TMTV Die Heater Representation



3.2.2.1 Recommended Test Parameters

The following example describes how to determine the voltage required to operate at the recommended MCH Thermal Design Power (TDP) listed in Table 2. The voltage to be applied to each heater can be easily calculated. The heater resistance must be measured on each TMTV unit to set the correct power dissipation. The typical resistance of the heater is 70 Ω. The maximum allowable power for the TMTV is 30 W so as not to exceed the temperature limit of the package.

Example

TDP = 8.1 W
R = 70 Ω (measured resistance across heater)
V = SQRT (Power x Resistance) = SQRT (8.1 W * 70 Ω) = 23.8 V

Solving for voltage, the calculated value of V = 23.8 V. Hence, if a nominal 23.8 V is applied to the die heater, the TMTV will operate at the 8.1 W thermal design power.

3.2.2.2 TMTV Correction Factors

Due to changes in die size between the TMTV and the planned production die size, a correction factor is required for any heatsink thermal performance measurements made with the TMTV. Thermal performance of a MCH heatsink is determined using the case-to-ambient thermal characterization parameter, Ψ_{CA} (Psi). Refer to Section 3.1 for instructions on measuring T_C (package case temperature). Figure 7 shows recommended ambient temperature measurement locations for a board in a JEDEC test configuration. Ψ_{CA} is analogous to thermal resistance but is defined using total package power instead of the actual power dissipated between the package case and local ambient. The TMTV die size is 8.153 mm x 8.153 mm [0.321 in x 0.321 in]. The correction factors listed in Table 5 are for a currently assumed die size of 9.73 mm x 9.73 mm [0.383 in x 0.383 in] for the MCH.

Table 5. TMTV Correction Factor

Parameter	Correction Factor
Ψ_{CA}	0.935

NOTE: The TMTV correction factor was calculated assuming an airflow velocity of 0.76 m/s [150 lfm] and a TIM comprised of phase change material. The correction factor may not apply to configurations that deviate from these assumptions.

Any case-to-ambient thermal characterization parameters based on data collected from a TMTV should be multiplied by the correction factor in Table 5 to account for changes in die size. The correction factor calculation is as follows:

$\{MCH\ \Psi_{CA}\} = \{TMTV\ \Psi_{CA}\}$ x Correction factor

Example Calculation

T_C = 90 °C
T_A = 50 °C
Total Package Power = 11.7 W
$\Psi_{CA,\ MEASURED} = (T_C - T_A)$ / Total Package Power = (90 – 50) / 11.7 = 3.4 °C/W

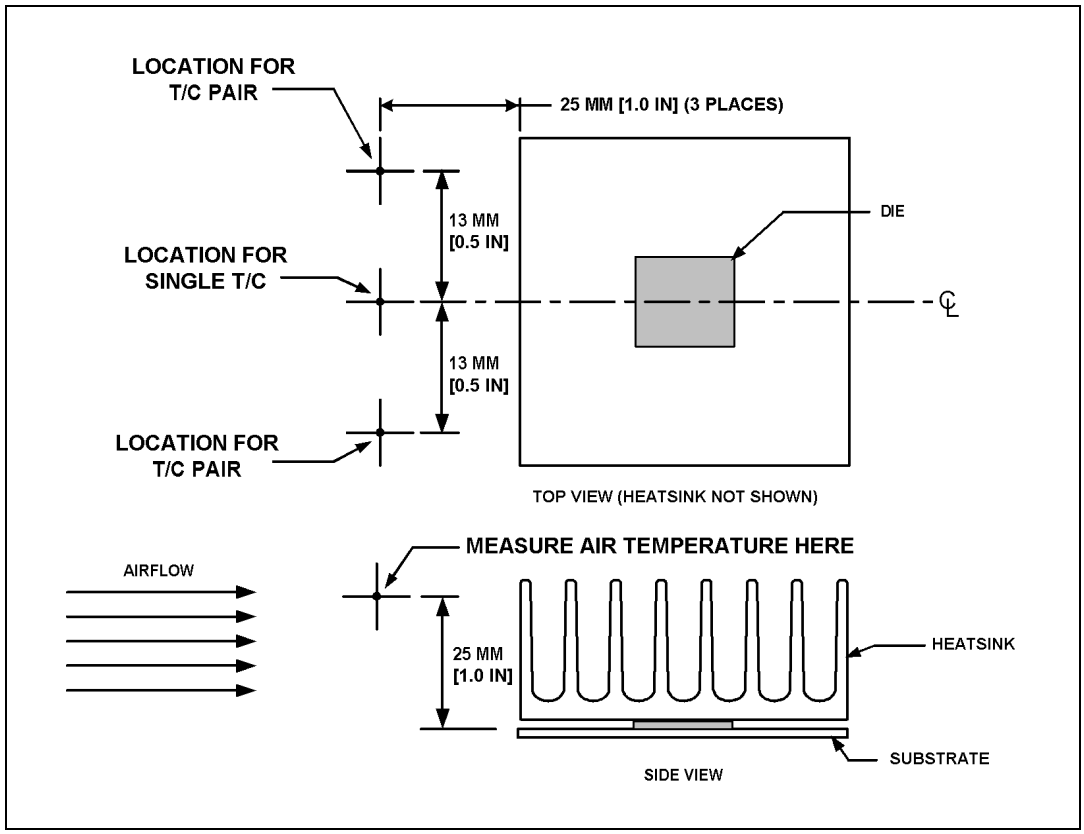
Applying the correction factor, we get:

$\Psi_{CA,\ CORRECTED}$ = Correction Factor x $\Psi_{CA,\ MEASURED}$ = 0.968 x 3.4 = 3.3 °C/W

3.3 Airflow Characterization

Figure 7 describes the recommended location for air temperature measurements measured relative to the component. For a more accurate measurement of the average approach air temperature, Intel recommends averaging temperatures recorded from two thermocouples spaced about 25 mm [1.0 in] apart. Locations for both a single thermocouple and a pair of thermocouples are presented.

Figure 7. Airflow Temperature Measurement Locations



Airflow velocity should be measured using industry standard air velocity sensors. Typical airflow sensor technology may include hot wire anemometers. Figure 7 provides guidance for airflow velocity measurement locations. These locations are for a typical JEDEC test setup and may not be compatible with chassis layouts due to the proximity of the processor to the MCH. The user may have to adjust the locations for a specific chassis. Be aware that sensors may need to be aligned perpendicular to the airflow velocity vector or an inaccurate measurement may result. Measurements should be taken with the chassis fully sealed in its operational configuration to achieve a representative airflow profile within the chassis.

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4 Reference Thermal Solution

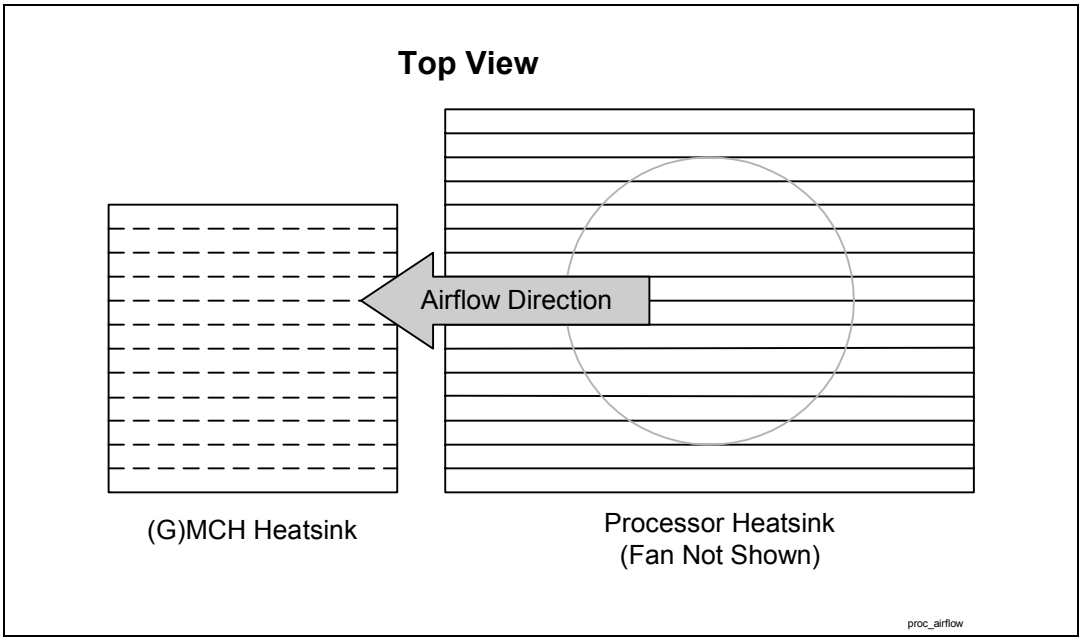
The Wave Solder Heatsink (WSHS) is the reference component thermal solution for the MCH. This chapter provides detailed information on operating environment assumptions, heatsink manufacturing, heatsink rework, and mechanical reliability requirements.

4.1 Operating Environment

An airflow speed of 0.76 m/s [150 lfm] is assumed to be present 25 mm [1 in] in front of the heatsink air inlet side of the attached reference thermal solution. The potential for increased airflow speeds may be realized by ensuring that airflow from the processor heatsink fan exhausts in the direction of the MCH heatsink. This can be achieved by orienting the processor heatsink fins perpendicular to the MCH heatsink face or by using a heatsink with omni directional airflow (e.g., a radial fin or "X" pattern heatsink). Figure 8 illustrates the fin orientation of a straight fin heatsink that provides airflow to the MCH heatsink. In addition, MCH board placement should ensure that the MCH heatsink is within the air exhaust area of the processor heatsink.

Note that heatsink orientation alone does not guarantee that 0.76 m/s [150 lfm] airflow speed will be achieved. The system integrator should use analytical or experimental means to determine whether a system design provides adequate airflow speed for a particular MCH heatsink.

Figure 8. Processor Heatsink Orientation to Provide Airflow to MCH Heatsink



Other methods exist for providing airflow to the MCH heatsink, including the use of system fans and/or ducting, or the use of an attached fan (active heatsink).

The local ambient air temperature (T_A) at the MCH heatsink is assumed to be 50 °C. The thermal designer must carefully select the location to measure airflow to get a representative sampling. These environmental assumptions are based on a 35 °C system external temperature measured at 1524 m [5000 ft].

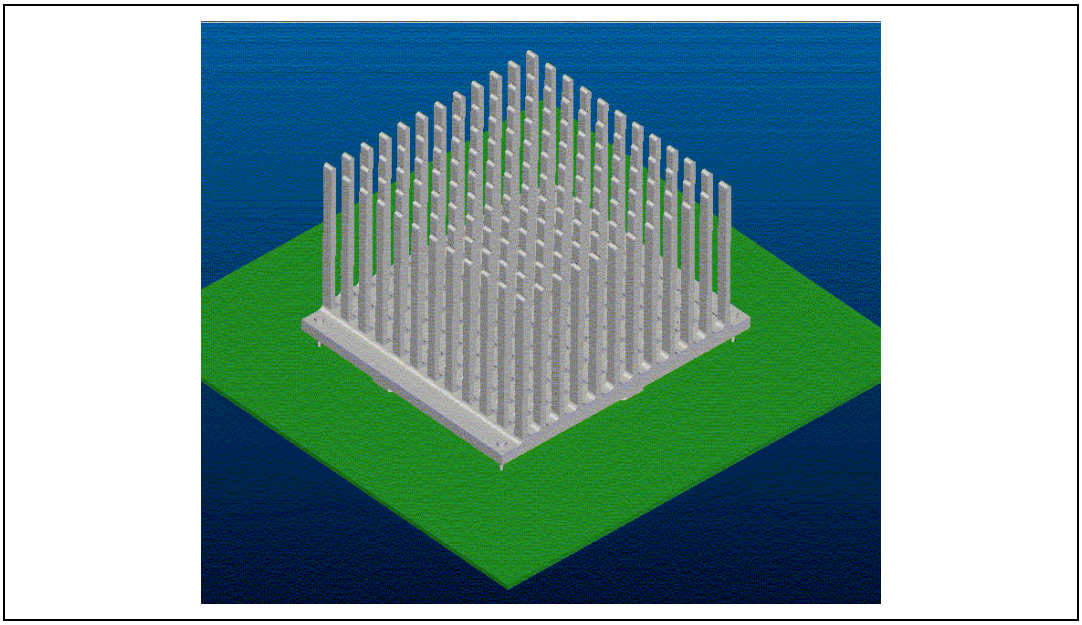
4.2 Mechanical Design Envelope

The motherboard component keep-out restrictions for the WSHS are included in Appendix B. The WSHS extends 38.2 mm [1.5 in] nominally above the board when mounted. System integrators should ensure no board or chassis components would intrude into the volume occupied by the WSHS.

4.3 Thermal Solution Assembly

The reference thermal solution consists of a passively cooled Wave Solder Heatsink. The heatsink consists of an extruded aluminum heatsink with four mounting pins pressed into each corner of the heatsink base. A thermal interface material (Chomerics T-710) is pre-applied to the heatsink bottom over an area in contact with the package die. A 45-degree dado cut is performed on the heatsink base to create rails to reduce the possibility of tilt when assembling the WSHS**. Since the rails are oriented at 45 degrees relative to the heatsink edges, the WSHS is only compatible with a MCH rotated 45 degrees relative to the motherboard.** Section 4.3.1 describes an alternate WSHS design that is compatible with a MCH that is not rotated relative to the motherboard. Note that the rails do not touch the package substrate in the nominal position. The WSHS is shown in the installed configuration in Figure 9 (the MCH cannot be seen in this view, as it is hidden by the WSHS base). Drawings of the WSHS extrusion and with the entire WSHS assembly are shown in Appendix B.

Figure 9. Wave Solder Heatsink Installed on Board



4.3.1 Alternate WSHS for Non-Rotated MCH

The WSHS can be modified into an alternate configuration for a non-rotated MCH. Customers that want to develop an alternate design should work with their suppliers and implement the following recommendations:

- Create an extrusion die that will create two parallel rails matching the rails shown in the heatsink drawing (Appendix B, Figure 16), but at a 0° rotation relative to the heatsink. The extruded rails should use the same width, height, and spacing as shown in the drawing. The tolerances shown should be replicated in the extrusion.
- Omit the dado cut from the manufacturing process.

4.3.2 Manufacturing with the WSHS

This section describes manufacturing related considerations for WSHS use in an HVM setting.

4.3.2.1 Assembly Process Settings

Table 6 provides recommended wave solder process settings for installation of the WSHS.

Table 6. Wave Solder Recommended Settings for WSHS

Setting	Minimum	Maximum	Notes
Board Temperature on Pre-heat Region Exit	90 °C [194 °F]	120 °C [248 °F]	Recommend not exceeding 120 °C [248 °F] due to flux dry out
Dwell Time	2.1 s	As Required	Not to exceed 160°C [320 °F] board topside temperature
Solder Bath Temperature	240 °C [464 °F]	As Required	Not to exceed 160°C [320 °F] board topside temperature using the minimum dwell time

In addition, the recommended solder type is standard eutectic 63/37 Sn/Pb. No “top hat” plungers should be used to hold down the WSHS during the wave solder process since it may increase the risk of heatsink tilt. For best results, the WSHS should be left in a “floating” condition as it passes through the wave solder.

4.3.2.2 Inspection Criteria

After the WSHS is installed and exits the wave solder process, it should be visually inspected to ensure there are no gross tilt issues. Any gross tilt in the WSHS will impact the thermal performance of the heatsink. The recommended allowable observed tilt is approximately 0.36 mm [0.014 in] variation between pin gaps on opposite sides of the heatsink (~16% difference in gap, nominal gap is ~2.2 mm [0.086 in]). The pin gap is defined as the distance between the bottom of the heatsink base and the top of the motherboard. This amount of gap is easily detectable by trained inspectors. Gross tilt inspection results can allow for closer inspection and measurement of tilt.

To establish the initial wave solder process, a more detailed inspection may be used to confirm the process is robust and does not induce heatsink tilt. A detailed inspection may include the use of “feeler” gauges to measure the pin gap more precisely and assess the presence of heatsink tilt. The recommended allowable tilt can be used as criteria for determining the success of the wave solder process. Once a successful wave solder process is in place, the manufacturer may choose to use visual gross tilt inspection in an HVM setting.

4.3.3 WSHS Removal and Installation Procedure

Two methods exist for WSHS removal, lead clipping or de-soldering. Re-installation of the heatsink for rework or metrology purposes includes a single method.

4.3.3.1 Removal via Lead Clipping Methodology

Recommended Equipment List

- 55-degree angle clippers (Figure 10)
- Solder wicking kit

Figure 10. 55-Degree Angle Clippers

Removal Procedure

1. Remove processor heatsink retention mechanism.
2. Cut the WSHS leads using the 55-degree angle clippers. To reduce potential of damaging board and components, cut the leads in the order shown in Figure 11.
3. Flip the board over and remove the leads, using tweezers and a soldering iron with a STTC 137 tip.
4. Apply flux and remove any residual solder from each hole.
5. Inspect the board and ensure all holes are clean and completely free of solder. Make sure none of the adjacent components were damaged during the removal process.

Figure 11. WSHS Lead Clipping Order

4.3.3.2 Removal via De-Soldering Methodology

Recommended equipment list

1. De-soldering gun
2. Solder wicking kit
3. Vertical rework jig (Figure 12)

Figure 12. Example Vertical Rework Jig

Removal Procedure

1. Remove processor heatsink retention mechanism.
2. De-solder the WSHS leads using a SMTC 104 tip. Use a small amount of solder to prime the tip if necessary.
3. Stand the board vertically using jig (Figure 12).
4. Use a soldering iron with an STTC 137 tip to loosen WSHS pins and remove the heatsink. Gently wiggle each lead loose while applying heat to lead.
5. Apply flux and remove any residual solder from each hole.
6. Inspect the board and ensure all holes are clean and completely free of solder. Make sure none of the adjacent components were damaged during the removal process.

4.3.3.3 Re-Installation Methodology

Recommended Equipment

- WSHS rework target
- SMT rework tool such as an SRT 1000 or 1100

Installation Procedure

1. Insert WSHS into board. Avoid scratching the board as the pins are placed into the mounting holes.
2. Ensure the WSHS "floats" on top of the MCH. The WSHS should move freely. If it does not "float," remove any residual solder that may be in the mounting holes.
3. Place the WSHS target on top of the WSHS fins.
4. Use the SMT rework tool to melt the TIM. Use 145 grams placement force and set the bottom temperature to 220 °C (428 °F) for 90 seconds duration.
5. Cool the board to room temperature.
6. Stand the board vertically using jig.
7. Solder the WSHS leads using a soldering iron with a STTC 137 tip.

Figure 13. WSHS Target

4.4 Environmental Reliability Requirements

The environmental reliability requirements for the reference thermal solution are shown in Table 7. These should be considered as general guidelines. Validation test plans should be defined by the user, based on anticipated use conditions and resulting reliability requirements.

Table 7. Reference Thermal Solution Environmental Reliability Requirements

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	• Quantity: 3 drops for + and - directions in each of 3 perpendicular axes (i.e., total 18 drops). • Profile: 50 G trapezoidal waveform, 11 ms duration, 4.3 m/s [170 in/s] minimum velocity change. • Setup: Mount sample board on test fixture. Include 450 g processor heatsink.	Visual\Electrical Check
Random Vibration	• Duration: 10 min/axis, 3 axes • Frequency Range: 5 Hz to 500 Hz • Power Spectral Density (PSD) Profile: 3.13 g RMS	Visual/Electrical Check
Thermal Cycling	• -40 °C to +85 °C, 1000 cycles	Visual Check
Temperature Life	• 85 °C, 1000 hours total	Visual/Electrical Check
Unbiased Humidity	• 85 % relative humidity / 130 °C, 100 hours	Visual Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 assemblies from 3 different lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

Appendix A: Enabled Suppliers

Enabled suppliers for the MCH WSHS reference thermal solution are listed in Table 8.

Table 8. MCH Wave Solder Heatsink Enabled Suppliers

Supplier	Intel Part Number	Vendor Part Number	Contact Information
CCI	C19335	00C852301A	Taiwan: Monica Chih, Project Manager, 886-2-29952666, Ext 131 USA: Harry Lin, 714-739-5797
Foxconn	C19335	2ZA41-001	Malaysia: Cheow-Kooi Lee, 604-6122122 USA: Kevin Tao, 714-626-1278

Note: These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

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Appendix B: Mechanical Drawings

The following table lists the mechanical drawings available in this document:

Figure 14. MCH Package Drawing

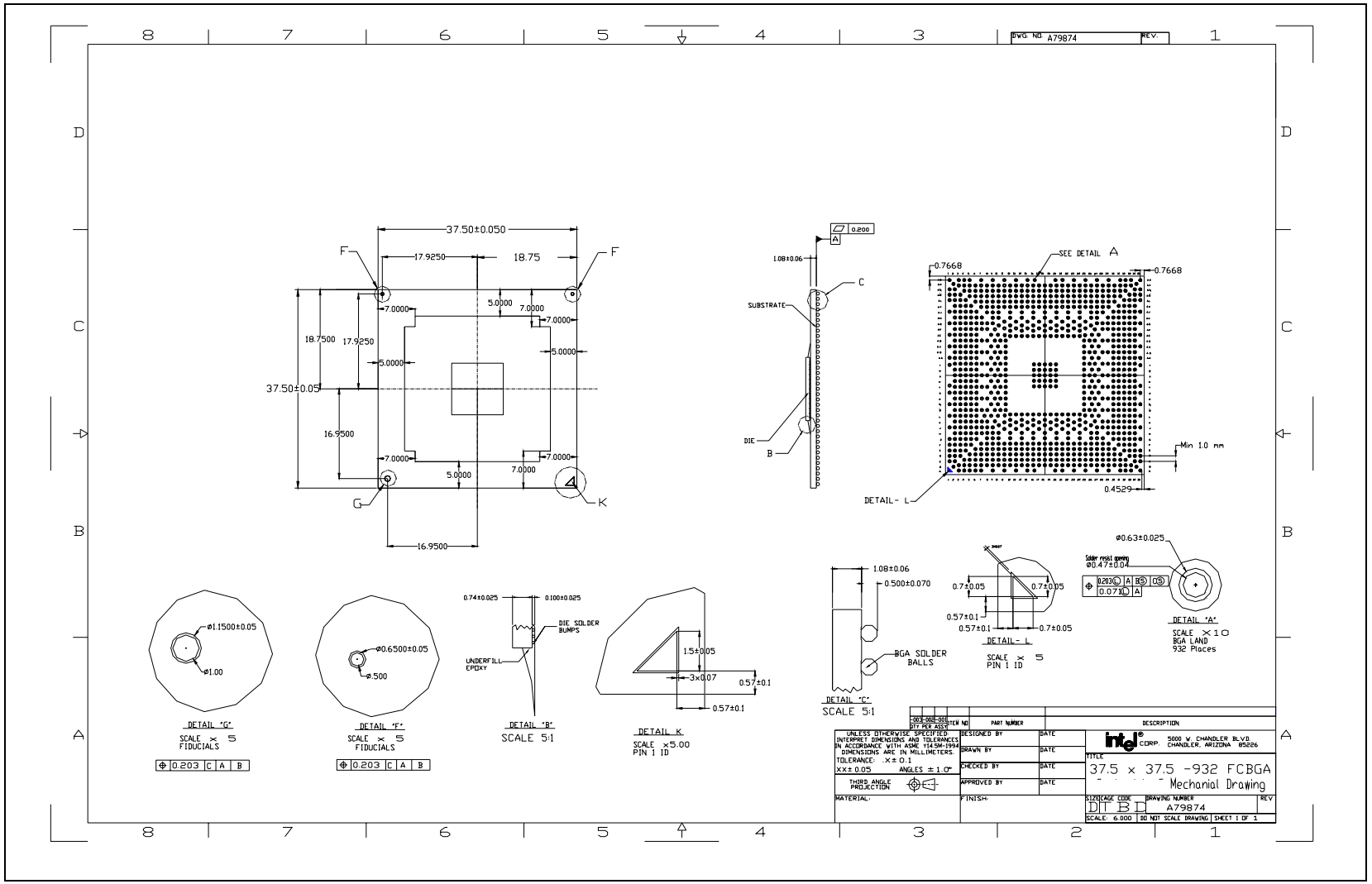

Figure 15. MCH Component Keep-Out Restrictions

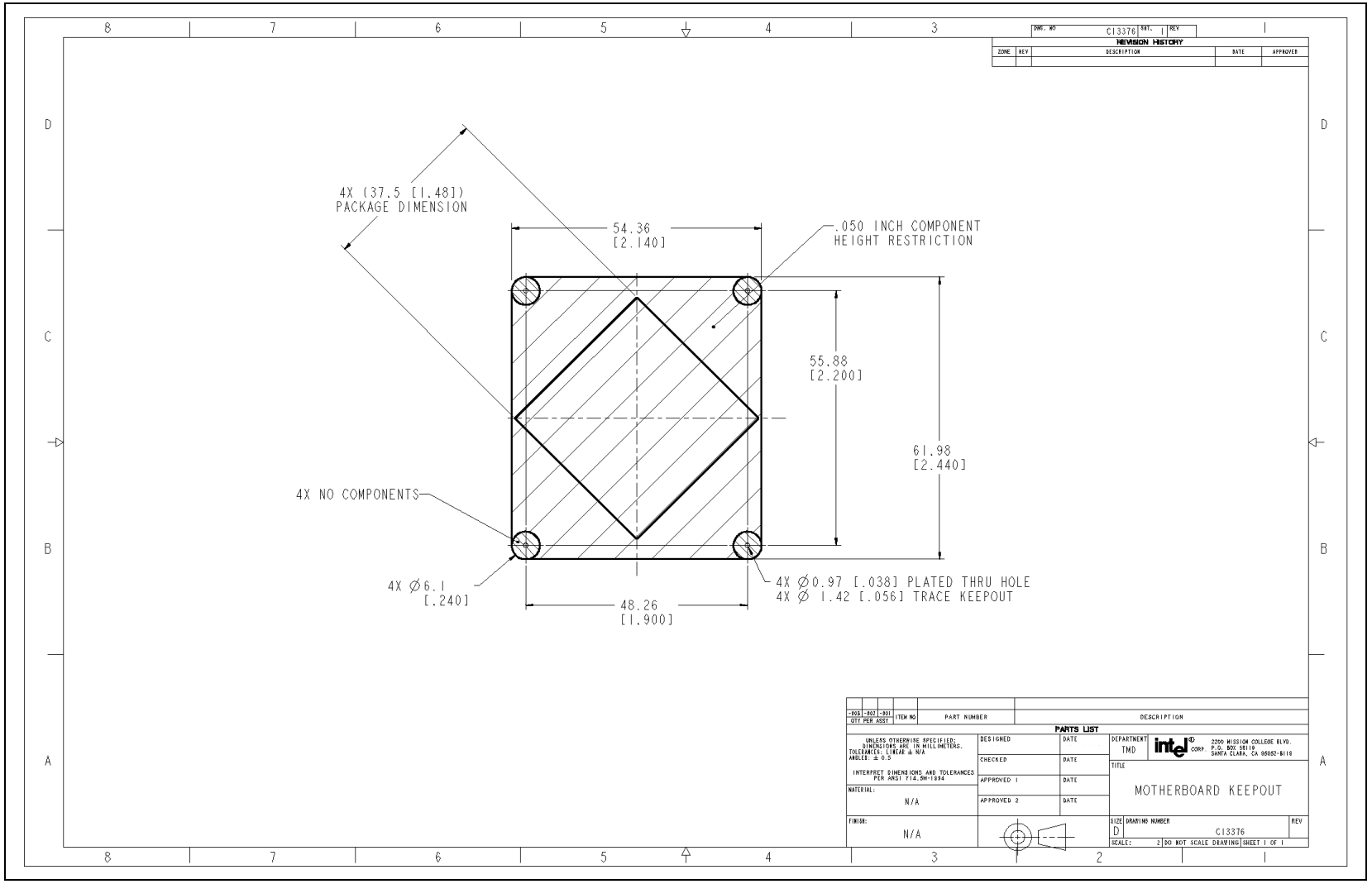

Figure 16. WSHS Heatsink Extrusion Drawing

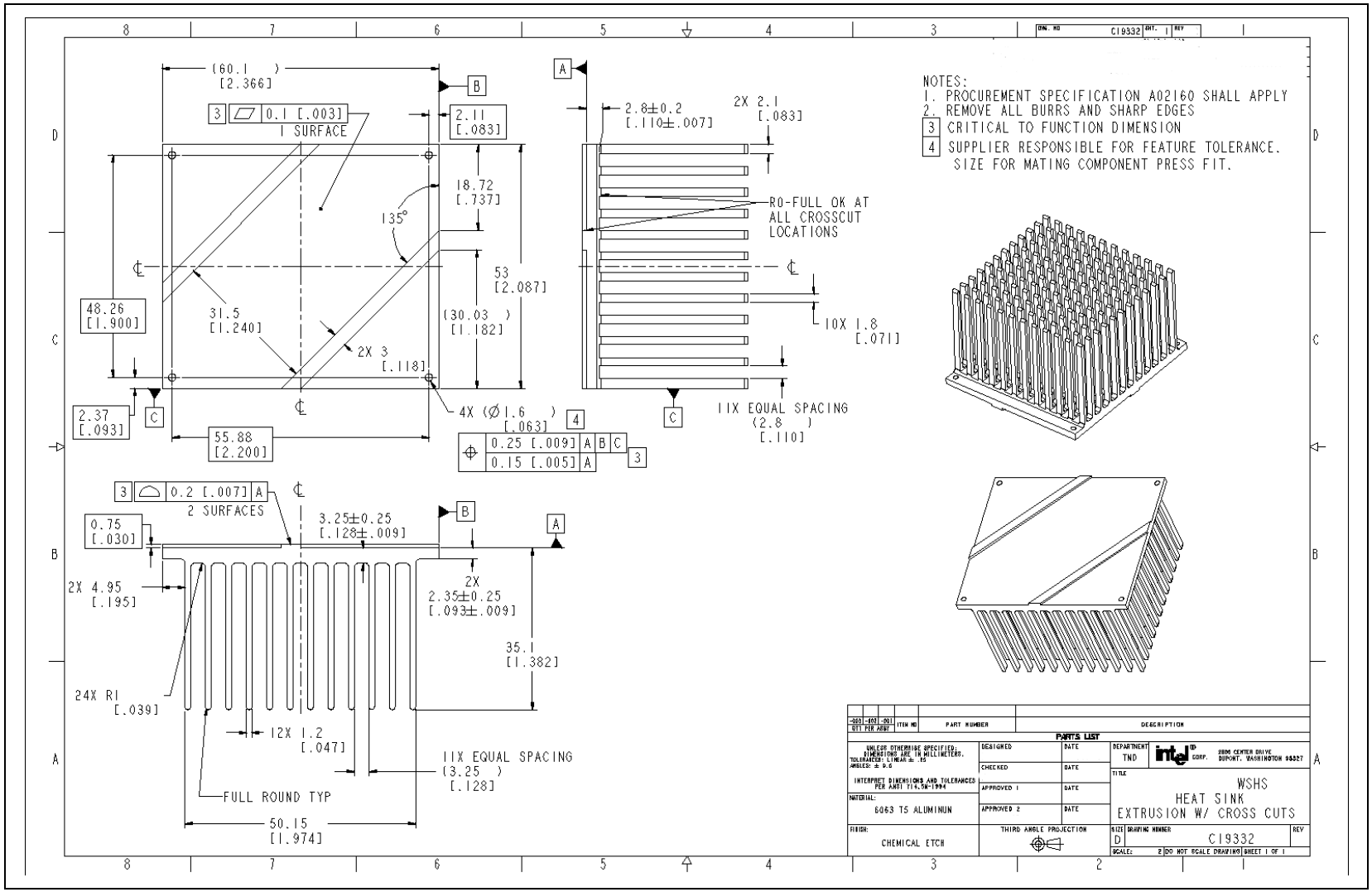

Figure 17. WSHS Heatsink Assembly Drawing